PIC32MX1XX/2XX/5XX 64/100-pin Family Silicon Errata and Data Sheet Clarification

The PIC32MX1XX/2XX/5XX 64/100-pin family devices that you have received conform functionally to the current Device Data Sheet (DS60001290**F**), except for the anomalies described in this document.

The errata described in this document will be addressed in future revisions of the PIC32MX1XX/2XX/5XX 64/100-pin family silicon.

Note: The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1 and Table 2. The last column of each table represents the latest silicon revision for the devices listed. If applicable, the silicon issues are summarized in Table 3.

Data Sheet clarifications and corrections, if applicable, start on page 10.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. Select *Window > Dashboard*, and then click the **Refresh Debug Tool Status** icon ( ).
5. The part number and the Device and Revision ID values appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various PIC32MX1XX/2XX/5XX 64/100-pin family silicon revisions are shown in Table 1 and Table 2.

TABLE 1: SILICON DEVREV VALUES FOR DEVICES WITH 256 KB OR 512 KB OF FLASH MEMORY

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)
		A0
PIC32MX150F256H	0x06A10053	0x0
PIC32MX150F256L	0x06A11053	
PIC32MX170F512H	0x06A30053	
PIC32MX170F512L	0x06A31053	
PIC32MX250F256H	0x06A12053	
PIC32MX250F256L	0x06A13053	
PIC32MX270F512H	0x06A32053	
PIC32MX270F512L	0x06A33053	
PIC32MX550F256H	0x06A14053	
PIC32MX550F256L	0x06A15053	
PIC32MX570F512H	0x06A34053	
PIC32MX570F512L	0x06A35053	

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001290**F**) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON DEVREV VALUES FOR DEVICES WITH 64 KB OR 128 KB OF FLASH MEMORY

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)	
		A0	A2
PIC32MX120F064H	0x06A50053	0x0	0x2
PIC32MX130F128H	0x06A00053		
PIC32MX130F128L	0x06A01053		
PIC32MX230F128H	0x06A02053		
PIC32MX230F128L	0x06A03053		
PIC32MX530F128H	0x06A04053		
PIC32MX530F128L	0x06A05053		

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001290**F**) for detailed information on Device and Revision IDs for your specific device.

TABLE 3: SILICON ISSUE SUMMARY

Module	Feature	Item	Issue Summary	Device Flash Memory (KB)	Affected Revisions	
					A0	A2
ADC	Differential Nonlinearity	1.	The ADC module is not within the published data sheet specification when operating at a conversion rate above 500 ksps.	64/128	X	X
				256/512	X	—
Clock	Clock Out	2.	A clock signal is present on the CLKO pin, regardless of the clock source and setting of the CLKO Enable Configuration bit, during a Power-on Reset (POR) condition.	64/128	X	X
				256/512	X	—
JTAG	Boundary Scan	3.	Boundary scan in not supported.	64/128	X	X
				256/512	X	—
Watchdog Timer	Windowed Watchdog	4.	Clearing the Watchdog Timer inside the window when in Window mode may cause a reset.	64/128	X	X
				256/512	X	—
USB	Idle Interrupt	5.	USB Idle interrupts cease if the IDLEIF flag is cleared and the bus is left idle for more than 3 ms.	64/128	X	X
				256/512	X	—
UART	Receive Overflow	6.	A receive FIFO overflow condition causes the shift register to stop receiving data and lose synchronization with the serial data stream.	64/128	X	X
				256/512	X	—
Comparator Voltage	—	7.	Some operational mode combinations of the Comparator Voltage Reference do not meet the data sheet specifications.	64/128	X	X
				256/512	X	—
Comparator Voltage Reference	—	8.	The Comparator Voltage Reference always behaves as if the CVRR bit is = 1, which specifies a range of 0 to 0.67 CVRSRC with a CVRSRC/24 step size.	64/128	X	X
				256/512	X	—
CTMU	Trigger	9.	The EDGEN bit generates a glitch on the CTED input causing a false trigger.	64/128	X	X
				256/512	X	—
CTMU	Module Operation	10.	The CTMU module is not functional.	64/128	X	
				256/512	X	—
ADC	IVREF	11.	The IVREF input to the ADC is not functional.	64/128	X	X
				256/512	X	—
HVD	HVDR	12.	On power-up, the High-Voltage Detect Reset event flag, HVDR bit in the RCON register, is being set.	64/128	X	X
				256/512	X	—
Power-Saving Modes	Idle	13.	On exit from Sleep mode, the SLEEP and IDLE status bits in the RCON register are being set.	64/128	X	X
				256/512	X	—
UART	Auto-baud	14.	Auto-baud does not function to set the baud rate.	64/128	X	X
				256/512	X	—
Bus Matrix	Flash Size	15.	The Flash Memory Size register (BMXPFMSZ) was not programmed with the correct value.	64/128	Date code pre-1750	
				256/512		

Legend: An 'X' indicates the issue is present in this revision of silicon;
shaded cells with an Em dash ('—') indicate that this silicon revision does not exist for this issue;
blank cells indicate an issue has been corrected or does not exist in this revision of silicon.

TABLE 3: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item	Issue Summary	Device Flash Memory (KB)	Affected Revisions	
					A0	A2
I/O Port	Drive Strength	16.	Pins RD15 & RF13 must be considered 4x Sink Driver Pins and not 8x Sink Driver Pins.	64/128	X	X
				256/512	X	—
I/O Port - Initial Pin State	Initial Pin State	17.	Random pin active output on power up.	64/128	X	X
				256/512	X	—
USB Low-Speed Mode	USB Low Speed	18.	USB Low-Speed Device and Host mode is not supported.	64/128	X	X
				256/512	X	—

Legend: An ‘X’ indicates the issue is present in this revision of silicon;
shaded cells with an Em dash (‘—’) indicate that this silicon revision does not exist for this issue;
blank cells indicate an issue has been corrected or does not exist in this revision of silicon.

Silicon Errata Issues

Note 1: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. The table provided in each issue indicates which issues exist for a particular revision of silicon based on Flash memory size.

2: The following applies to the Affected Silicon Revision tables in each silicon issue:

- An 'X' indicates the issue is present in this revision of silicon
- Shaded cells with an Em dash ('—') indicate that this silicon revision does not exist for this issue
- Blank cells indicate an issue has been corrected or does not exist in this revision of silicon.

1. Module: ADC

When the ADC is configured for 10-bit operation, the specifications in the data sheet are not met for operation above 500 ksps.

Work around

For 600 ksps operation, RIN = 500 ohms, TSAMP = 2 TAD. The module specifications are shown in Table 4. For 1000 ksps operation, RIN = 200 ohms, TSAMP = 2 TAD. The module specifications are shown in Table 5.

TABLE 4: 600 KSPS OPERATION

Parameter No.	Symbol	Minimum	Typical	Maximum	Units
AD17	RIN	—	—	200	Ohm
ADC Accuracy – Measurements taken with External VREF+/VREF-					
AD21c	INL	-1.5	—	1.5	LSB
AD22c	DNL	-1.4	—	2.1	LSB
AD23c	GERR	-1.2	—	1.2	LSB
ADC Accuracy – Measurements taken with Internal VREF+/VREF-					
AD21d	INL	-1.5	—	1.5	LSB
AD22d	DNL	-1.4	—	2.1	LSB

TABLE 5: 1000 KSPS OPERATION

Parameter No.	Symbol	Minimum	Typical	Maximum	Units
AD17	RIN	—	—	200	Ohm
ADC Accuracy – Measurements taken with External VREF+/VREF-					
AD21c	INL	-5.2	—	6.5	LSB
AD22c	DNL	-3.4	—	7	LSB
AD23c	GERR	-1.5	—	1.5	LSB
ADC Accuracy – Measurements taken with Internal VREF+/VREF-					
AD21d	INL	-5.2	—	6.5	LSB
AD22d	DNL	-3.4	—	7	LSB

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2			
64/128	X	X			
256/512	X	—			

2. Module: Clock

A clock signal is present on the CLKO pin, regardless of the clock source and setting of the CLKO Enable Configuration bit, OSCIOFNC (DEVCFG1<10>), during a Power-on Reset (POR) condition.

Work around

Do not connect the CLKO pin to a device that would be adversely affected by rapid pin toggling or a frequency other than that defined by the oscillator configuration. Do not use the CLKO pin as an input if the device connected to the CLKO pin would be adversely affected by the pin driving a signal out.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2			
64/128	X	X			
256/512	X	—			

3. Module: JTAG

Boundary Scan is not supported.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2			
64/128	X	X			
256/512	X	—			

4. Module: Watchdog Timer

When the Watchdog Timer module is used in Windowed mode, the module may issue a reset even if the user tries to clear the module within the allowed window.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2			
64/128	X	X			
256/512	X	—			

5. Module: USB

If the bus has been idle for more than 3 ms, the IDLEIF interrupt flag is set. If software clears the interrupt flag and the bus remains idle, the IDLEIF interrupt flag will not be set again.

Work around

Software can leave the IDLEIF bit set until it has received some indication of bus resumption (i.e., Resume, Reset, SOF, or Error).

Note:	Resume and Reset are the only interrupts that should be following IDLEIF assertion. If the IDLEIF bit is set, it should be okay to suspend the USB module (as long as this code is protected by the GUARD and/or ACTPEND logic). This will require software to clear the IDLEIF interrupt enable bit to exit the USB ISR (if using interrupt driven code).

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2			
64/128	X	X			
256/512	X	—			

6. Module: UART

During receive FIFO overflow conditions, the shift register stops receiving data, which causes the UART to lose synchronization with the serial data stream.

The only way to recover from this condition is to turn the UART OFF and ON until it synchronizes. This could require several OFF/ON sequences.

Work arounds

Work around 1:

Avoid the RX overrun condition by ensuring that the UARTx module has a high enough interrupt priority such that other peripheral interrupt processing latencies do not exceed the time to overrun the UART RX buffer based on the application baud rate. Alternately or in addition to, set the URXISEL bits in the UxSTA register to generate an earlier RX interrupt based on RX FIFO fill status to buy more time for interrupt latency processing requirements.

Work around 2:

If avoiding RX FIFO overruns is not possible, implement a ACK/NAK software handshake protocol to repeat lost packet transfers after restoring UART synchronization.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2			
64/128	X	X			
256/512	X	—			

7. Module: Comparator Voltage

Three of the four Comparator Voltage Reference operational modes, defined in Table 6, do not meet data sheet specifications.

TABLE 6:

CVRCON <CVRSS>	CVRCON <CVRR>	Accuracy Specification	Actual Accuracy
0 = (AVDD/AVSS)	0 = (CVRSRC/32)	0.5 LSB	8.2 LSB
0 = (AVDD/AVSS)	1 = (CVRSRC/24)	0.25 LSB	0.34 LSB
1 = (VREF+/VREF-)	0 = (CVRSRC/32)	0.5 LSB	8.2 LSB

Work around

If possible, set both the CVRSS bit (CVRCON<4>) and the CVRR bit (CVRCON<5>) to '1', which specifies the Comparator Voltage Reference source CVRSRC = [(VREF+) - (VREF-)] and 0 to 0.67 CVRSRC with a step size of CVRSRC/24, respectively.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2			
64/128	X	X			
256/512	X	—			

8. Module: Comparator Voltage Reference

The Comparator Voltage Reference always behaves as if the CVRR bit (CVRCON<5>) is equal to '1', which specifies a range of 0 to 0.67 CVRSRC with a step size of CVRSRC/24, instead of a range of 0.25 to 0.75 CVRSRC and a step size of CVRSRC/32.

Work around

If possible, set the CVRR bit (CVRCON<5>) = 1 (i.e., 0 to 0.67 CVRSRC, with CVRSRC/24 step size, respectively).

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2			
64/128	X	X			
256/512	X	—			

9. Module: CTMU

The EDGEN bit generates a glitch on CTED input causing a false trigger.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2			
64/128	X	X			
256/512	X	—			

10. Module: CTMU

The CTMU module is not functional.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2			
64/128	X				
256/512	X	—			

11. Module: ADC

Converting the Internal Band Gap (IV_{REF}) voltage source generates a High-Voltage Detect (HVD) event and aborts the conversion; therefore, this feature is not functional.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2			
64/128	X	X			
256/512	X	—			

12. Module: HVD

On power-up, the High-Voltage Detect Reset, event flag (HVDR bit in the RCON register) is set incorrectly.

On a power-up, only the POR, BOR, and EXTR bits should be set with the proper V_{CAP} bypass capacitor value, as stated in the current data sheet.

Work around

Check the status of the POR bit in the RCON register when checking the HVDR bit. If the POR bit is set, both bits can be cleared as the HVDR bit is a false detection. If the POR bit is clear, the HVDR bit has been correctly detected and can be handled according to the requirements of the application.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2			
64/128	X	X			
256/512	X	—			

13. Module: Power-Saving Modes

On exit from Sleep mode, both the SLEEP and IDLE status bits in the RCON register are set.

Work around

Add the following code to the user application at the point it wakes from Sleep mode:

```
rcon_var1 = RCON;
// ... enter Sleep mode
if (rcon_var1 & 0x4) Nop();
// If IDLE bit already set previously
// before sleep do nothing
else RCONbits.IDLE = 0x0;
// If IDLE bit is not set previously
// and is after Sleep mode then clear
```

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2			
64/128	X	X			
256/512	X	—			

14. Module: UART

The UART auto-baud feature is intended to set the baud rate during run time based on external data input. However, this feature does not function.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2			
64/128	X	X			
256/512	X	—			

15. Module: Bus Matrix

The Flash Memory Size register (BMXPFMSZ) was not programmed with the correct value.

Work around

Use a fixed number based on the size of the part being used.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2			
64/128	Date code pre-1750				
256/512					

16. Module: I/O Port

RD15 & RF13 should be considered 4x Sink Driver Pins and not 8x Sink Driver Pins. See Parameter DO10, DO20, and DO20A in the data sheet.

Work around

None.

Affected Silicon Revisions

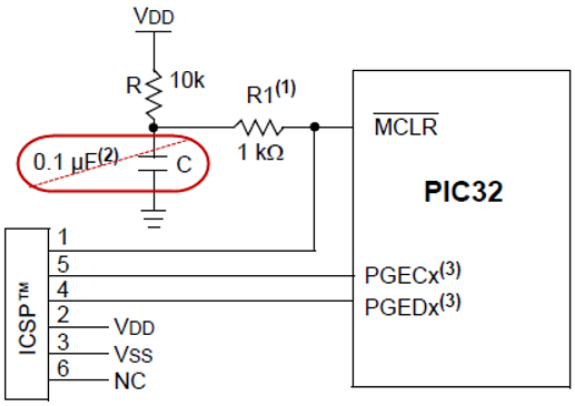
Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2			
64/128	X	X			
256/512	X	—			

17. Module: I/O Port - Initial Pin State

On power-up depending on the VDD ramp rate, the I/O pins can be in an active random output driving state if MCLR is active until a BOR event.

Work around 1:

If, not using an external reset supervisor IC or equivalent, remove the MCLR capacitor as shown below, and retain the MCLR Pull-up resistor.



Work around 2:

If using an external reset supervisor IC or equivalent, increase the value of the VCAP capacitor to ≥47 µf ceramic or solid tantalum capacitor with an ESR ≤ 1 ohm.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2			
64/128	X	X			
256/512	X	—			

18. Module: USB Low-Speed Mode

USB Low-Speed mode is not functional in both Device and Host modes due to signal integrity compliance issues.

Work around 1:

Use USB Full-Speed mode.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision				
	A0	A2			
64/128	X	X			
256/512	X	—			

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001290**F**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

APPENDIX A: REVISION HISTORY

Rev A Document (10/2014)

Initial release of this document, issued for revision A0 silicon, which includes silicon issues 1 (ADC), 2 (Clock), 3 (JTAG), 4 (Watchdog Timer), 5 (USB), 6 (UART), 7 (Comparator Voltage), 8 (Comparator Voltage Reference), 9 (CTMU), 10 (CTMU) and 11 (ADC).

Rev B Document (7/2015)

Updated silicon issues 6 (UART) and 11 (ADC).

Added silicon issues 12 (HVD) and 13 (Power-Saving Modes).

Rev C Document (4/2016)

Revised document for silicon revisions A2.

Added silicon issue 14 (UART).

Modified Silicon DEVREV Value Table 1 and added Silicon DEVREV Value Table 2.

Updated the Silicon Issue Summary table (Table 3) and silicon issue 9 (CTMU).

Updated all Affected Silicon Revision tables.

Rev D Document (6/2018)

Added silicon issue 15 (Bus Matrix).

Rev E Document (8/2018)

Added Silicon Issue 16 (**16. Module:I/O Port**).

Revision F Document (08/2019)

Added Data Sheet Clarification .

Revision G Document (01/2020)

Added silicon issues **17. Module:I/O Port - Initial Pin State** and **18. Module:USB Low-Speed Mode**.

Revision H Document (04/2020)

Clarified Silicon Issues **17. Module:I/O Port - Initial Pin State** and **18. Module:USB Low-Speed Mode** to denote the lack of a Revision A2 silicon for devices with 256/512 KB Device Flash Memory.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Trademarks

ISBN: 978-1-5224-5945-3

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4485-5910
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820